Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A pattern layout method of a semiconductor made in one chip with an anode driver, a cathode driver, and memory portions comprising:

laying out drivers connected to the memory portions equally in the chip, said drivers include a plurality of output regions; ~~and~~

arranging each memory portion equally in a vicinity of each of the drivers; and

forming a dummy pattern adjacent an output bit group and having a shape equivalent to the output regions.

2. (Previously Presented) The pattern layout method according to claim 1, wherein desired drivers connected to the memory portions are divided into plural groups and each of the memory portions is provided in every group.

3. (Previously Presented) The pattern layout method according to claim 1, wherein the drivers connected to the memory portions are placed face to face at right and left positions or top and bottom positions, and each memory portion is arranged at a center portion of the chip.

4. (Currently Amended) The pattern layout method according to claim 1, wherein the plurality of output regions constitute [[an]] the output bit group, and each output region corresponds to one bit~~, and the method further comprises forming a dummy pattern adjacent to the output bit group and having a shape equivalent to the output region~~.

5. (Previously Presented) The pattern layout method according to claim 4, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bit groups are arranged.

6. (Currently Amended) The pattern layout method according to claim 4, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent to each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent [[to]] each other.

7. (Previously Presented) The pattern layout method according to claim 4, wherein the dummy pattern has a shape equivalent to a wiring for gate electrode.

8. (Canceled)

9. (Canceled)

10. (Currently Amended) A pattern layout method of a semiconductor device constituting drivers for driving display where drivers, memory portions are made in one chip, the drivers arranging plural output regions corresponding to one bit to constitute output bit groups, the method comprising:

arranging the drivers at periphery portion in the chip in a state of grouping by every desired output bit group; and

arranging wirings connected to each output bit group of the drivers, the wirings are disposed peripherally to circle around within the chip; and

forming a dummy pattern adjacent the output bit groups and having a shape equivalent to the output regions.

11. (Previously Presented) The pattern layout method according to claim 19,

wherein the drivers includes an anode driver and a cathode driver, and the drivers are arranged at periphery portions in the chip in a state that one of the anode driver and the cathode driver is grouped by every desired output bit group.

12. (Previously Presented) The pattern layout method according to claim 19, wherein the wirings include a power source line and a signal line.

13. (Currently Amended) The pattern layout method according to claim 19 wherein each of the output bit groups ~~surround~~ surrounds ~~the~~ memory portions.

14. (Canceled).

15. (Currently Amended) The pattern layout method according to claim [14] 10, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are disposed.

16. (Currently Amended) The pattern layout method according to claim [14] 10, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent to each other is less than the number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent [[to]] each other.

17. (Currently Amended) The pattern layout method according to claim [14] 10, wherein the dummy pattern has a shape equivalent to a wiring for gate electrode.

18. (Currently Amended) A pattern layout method for a semiconductor chip comprising:

laying out an anode driver and a cathode driver equally in the semiconductor chip, each of said drivers containing a plurality of output regions constituting an output bit group, and each output region corresponding to one bit;

providing a memory portion for each of the drivers; and

forming a dummy pattern adjacent [[to]] the output bit group, said dummy pattern having a shape equivalent to the output region.

19. (Currently Amended) A pattern layout method for a semiconductor chip comprising:

disposing drivers at periphery portions of the semiconductor chip, each driver with a plurality of output regions, which constitutes an output bit group, and said output region corresponding to one bit; ~~and~~

providing wirings for connecting each output bit group of the ~~devices~~ drivers, the wirings are peripherally disposed to circle around within the chip; and

forming a dummy pattern adjacent the output bit groups and having a shape equivalent to the output regions.

20. (Previously Presented) The pattern layout method according to claim 19, further comprising:

providing memory portions approximately in the center of the semiconductor chip.